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| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
|---|---|---|---|---|
| 10/003,180 | 10/30/2001 | Heon-Deok Park | 9898-197 | 4103 |

7590 03/16/2004

MARGER JOHNSON & McCOLLOM, P.C.
1030 S.W. Morrison Street
Portland, OR 97205

| EXAMINER | |
|---|---|
| KERVEROS, JAMES C | |
| ART UNIT | PAPER NUMBER |
| 2133 | |

DATE MAILED: 03/16/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 10/003,180 | PARK ET AL. | |
| | Examiner | Art Unit | |
| | James C Kerveros | 2133 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *05 March 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *30 October 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date 3.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

## DETAILED ACTION

### *Specification*

The abstract of the disclosure is objected to because it does not comply with the proper language and format. The Applicant should avoid using phrases, throughout the abstract, such as "according to various aspects and embodiments of this invention", "provided", "preferably", "can include" should be changed to includes, "pattern memory can be used to store" should be "pattern memory stores"

Correction is required. See MPEP § 608.01(b).

Applicant is reminded of the proper language and format for an abstract of the disclosure.

The abstract should be in narrative form and generally limited to a single paragraph on a separate sheet within the range of 50 to 150 words. It is important that the abstract not exceed 150 words in length since the space provided for the abstract on the computer tape used by the printer is limited. The form and legal phraseology often used in patent claims, such as "means" and "said," should be avoided. The abstract should describe the disclosure sufficiently to assist readers in deciding whether there is a need for consulting the full patent text for details.

The language should be clear and concise and should not repeat information given in the title. It should avoid using phrases which can be implied, such as, "The disclosure concerns," "The disclosure defined by this invention," "The disclosure describes," etc.

### *Claim Rejections - 35 USC § 102*

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1-20 are rejected under 35 U.S.C. 102(b) as being anticipated by Conner (US 5794175), issued August 11, 1998.

Regarding Claims 1, 8, 12 and 16-20, Conner discloses an automatic system for testing semiconductor device memory chips in parallel, comprising:

A plurality of comparator and driver units, such as a driver/comparator pair made up of a driver 330(1) and a comparator 332(1), FIG. 3A, where each driver 330(1) drives an input signal pattern from Pattern generator (118, FIG. 1) to be applied on each data line 312(1) corresponding to input pins of the semiconductor device DUT array 12, FIG. 2, and where each comparator 332(1), which is a "dual comparator", compares the data output from the output pins of the semiconductor device DUT array 12 with a predetermined output signal pattern, for indicating whether the output data bit result is HI or LO.

A plurality of control units, such as set of address lines for each row 310(1) and column control line 340(1) configured to electrically connect a corresponding driver 330(1) and a comparator 332(1), to a pin of the semiconductor device DUT array 12, in response to a control signal, wherein pins of the semiconductor device are divided into pin groups, corresponding to a set of data lines, such as 312(1) where each set of data lines has 20 lines, and where each pin group has K=20 number of pins, where K is an integer greater than 1. A pattern memory for storing the input signal patterns and the output signal patterns, located in the tester 112, which contains pattern generator 118 which further generates the pattern of test signals that tests each DUT array 12.

Regarding Claims 2 and 3, Conner discloses Multiplexer 336 for selecting the columns through control line 340(1) via a data bus, corresponding to locations in array 212 as shown in FIG. 3A.

Regarding Claim 4, Conner discloses output memory located in work station (110, FIG. 1), such as a PC computer having memory, for storing the results of the error processor 124 from the appropriate devices under test 116.

Regarding Claims 5-7, 9-11, and 13-15, Conner discloses an input pattern memory located in work station (110, FIG. 1) for storing the test patterns for the pattern generator 118 and an output memory located in work station (110, FIG. 1), such as a PC computer having memory, for storing the results of the error processor 124 from the appropriate devices under test 116.

***Conclusion***

Any inquiry concerning this communication or earlier communications from the examiner should be directed to James C Kerveros whose telephone number is (703) 305-1081. The examiner can normally be reached on 9:00 AM TO 5:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Albert Decady can be reached on (703) 305-9595. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

U.S. PATENT OFFICE
Examiner's Fax: (703) 746-4461
Email: james.kerveros@uspto.gov

Date: 12 March 2004
Office Action: Non-Final Rejection

By: _____

James C Kerveros
Examiner
Art Unit 2133

Guy J. Lamarre
for

Albert DeCady
Primary Examiner